CLAIMS

1. A process for forming a dual metal gate structure, comprising:

    providing a semiconductor substrate having a first region and a second region, wherein the first region has a first conductivity type and the second region has a second conductivity type, different from the first conductivity type;

    forming a dielectric layer overlying the first region and the second region of the semiconductor substrate;

    forming an etch stop layer overlying the first and second regions;

    forming a first metal-containing layer overlying the dielectric layer and the etch stop layer, wherein the first metal-containing layer overlies the first region of the semiconductor substrate;

    forming a second metal-containing layer overlying the first metal-containing layer, the dielectric layer, and the etch stop layer;

    forming a patterned masking layer overlying the second metal-containing layer; and

    dry etching the first and second metal-containing layers using the patterned masking layer to form a first gate electrode over the first region and a second gate electrode over the second region.

2. The process of claim 1, wherein one of the first and second metal-containing layers has a work function of at least 4.6 electron volts (eV) and the other one of the first and second metal-containing layers has a work function of at most 4.4 eV.

3. The process of claim 1, wherein one of the first and second metal-containing layers comprises titanium nitride (TiN) and another one of the first and second metal-containing layers comprises tantalum silicon nitride (TaSiN).

4. The process of claim 3, wherein the etch stop layer comprises hafnium oxide.

5. The process of claim 4, wherein the dielectric layer comprises silicon oxynitride.

6. The process of claim 5, wherein the first metal-containing layer is TiN, the second metal-containing layer is TaSiN, the first conductivity type of the first substrate region is N-type, and second conductivity type of the second substrate region is P-type.

7. The process of claim 6 wherein the TaSiN overlies the first and second substrate regions.

8. The process of claim 7, further comprising:

forming a silicon-containing layer overlying the second metal-containing layer, wherein the patterned masking layer overlies the silicon-containing layer;

dry etching the silicon-containing layer using the patterned masking layer;

forming an anti-reflective coating (ARC) layer overlying the silicon-containing layer, wherein the patterned masking layer overlies the ARC layer; and

dry etching the ARC layer using the patterned masking layer.

9. The process of claim 8, further comprising:

forming doped regions in the first and second regions of the semiconductor substrate, adjacent the first and second gate stacks, and forming sidewall spacers adjacent the first and second gate stacks to form a first transistor and a second transistor.

10. The process of claim 1, wherein the gate dielectric layer is formed in direct contact with the substrate and the etch stop layer is formed directly on the gate dielectric layer.

11. The process of claim 10, wherein the gate dielectric is thermally grown.

12. The process of claim 1, where the etch stop layer is formed in direct contact with the substrate and the gate dielectric layer is formed directly on the etch stop layer and wherein the gate dielectric layer is a deposited film.

13. The processing of claim 1, wherein the dielectric layer comprises a dielectric having a dielectric constant (K) of at least 3.9.

14. The process of claim 1, wherein the etch stop layer comprises a material selected from a metal oxide, metal silicate, and metal aluminate.

15. A process for forming a dual metal gate structure, comprising:

forming an etch stop layer and a gate dielectric layer overlying first and second regions of a substrate, the first and second regions having different conductivity types;

forming a first metal-containing layer overlying and in contact with an upper layer of the etch stop layer and the gate dielectric layer over a first region of the substrate;

forming a second metal-containing layer after forming the first metal-containing layer, the second metal-containing layer being in contact with the first metal-containing layer overlying the first region and in contact with the upper layer of the etch stop layer and the gate dielectric layer overlying the second region;

etching the first and second metal-containing layers during formation of first and second gate stacks using at least one halogen-based etchant to etch the first and second metal layers, wherein the etchant is selective to the etch stop layer such that the etch stop layer prevents the etchant from etching into the second region of the substrate.

16. The process of claim 15, wherein the etch stop layer is hafnium oxide, the dielectric layer is silicon oxynitride, the first region is N type, the second region is P-type, the first metal-containing layer is TiN, the second metal containing layer is TaSiN, and the etchant includes chlorine and a fluorine based compound.

17. The process of claim 15, wherein the gate dielectric layer comprises the upper layer of the gate dielectric layer and the etch stop layer.

18. A process for forming a dual metal gate structure comprising:

providing a semiconductor substrate having an N-doped region and a P-doped region;

forming a dielectric layer and etch stop layer overlying the semiconductor substrate;

forming a first gate stack overlying the N-doped region, the first gate stack having a first metal-containing gate electrode overlying and in physical contact with the upper layer of the dielectric layer and etch stop layer wherein forming the first gate stack comprises dry etching a first metal-containing layer to form the first metal-containing gate electrode; and

forming a second gate stack overlying the P-doped region, the second gate stack having a second metal-containing gate electrode overlying and in physical contact with the higher of the dielectric layer and the etch stop layer, wherein forming the second gate stack comprises dry etching a second metal-containing layer to form the second metal-containing gate electrode, and wherein the first metal-containing gate electrode has a first work function and the second metal-containing gate electrode has a second work function, different from the first work function.

19. The process of claim 18, wherein one of the first and second work functions is at least 4.6 eV and another one of the first and second work functions is at most 4.4 eV.

20. The process of claim 18, wherein the etch stop layer is selected from a metal oxide, metal silicate, and metal aluminate.

21. The process of claim 20, wherein the first and metal-containing gate electrodes comprises titanium nitride and the second metal-containing gate electrode comprises tantalum silicon nitride.

22. The process of claim 21, wherein the gate dielectric comprises silicon, oxygen, and nitrogen.

23. The process of claim 22, wherein the gate dielectric is the upper of the gate dielectric layer and the etch stop layer.

24. The process of claim 22, wherein the etch stop layer is the upper of the gate dielectric layer and the etch stop layer.